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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. In other documentation, to reduce potential confusion, the only change to product numbers and names has been in the company name prefix: where a product number/name was HP XXXX the current name/number is now Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

User's Guide

Publication number E2466-97006
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For Safety information, Warranties, and Regulatory information, see the pages behind Appendix A

HP E2466C Preprocessor Interface for the Intel Pentium® II Processor

The HP E2466C Preprocessor Interface—At a Glance

The HP E2466C Preprocessor Interface, when used together with the HP 16505A Prototype Analyzer, provides a complete interface for state or timing analysis between any Intel Pentium® II processor target system and the HP logic analyzers listed below. The HP E2466C Preprocessor Interface requires that the logic analyzer module is in an HP 16500B/C mainframe; the HP 16505A Prototype Analyzer is also required.

The inverse assembler provides Pentium II processor assembly language mnemonics and accurate instruction execution tracking of up to four processors. The inverse assembler also supports Intel's MMX™ Technology. The HP E2467A APIC Bus Preprocessor Interface can also be used with the HP E2466C Preprocessor Interface to provide simultaneous bus analysis.

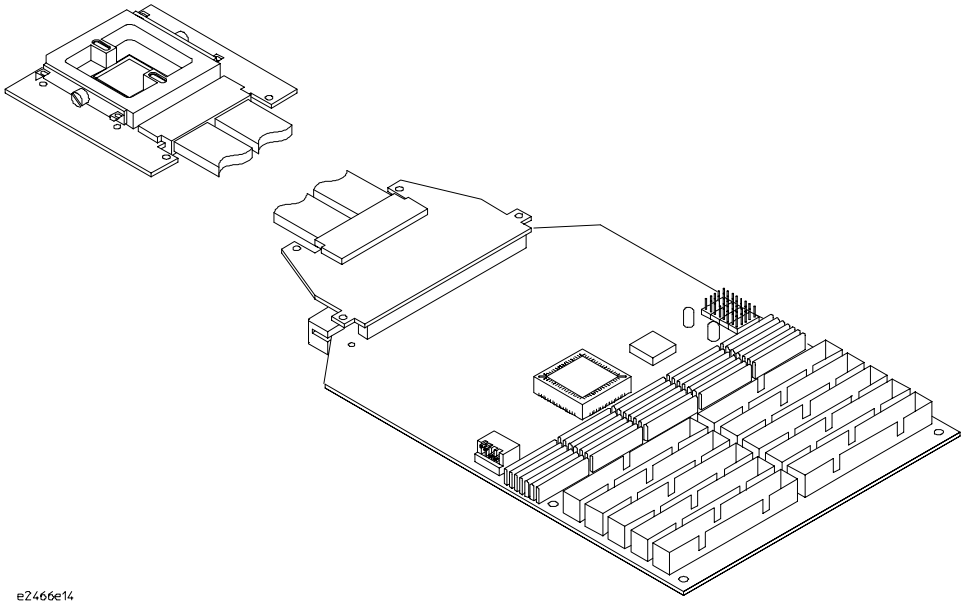
For instruction disassembly, Branch Trace Messages must be enabled and caches must be disabled. This requires a Pentium II processor run-control tool (such as the HP E3493A) and a 30-pin debug port on the target system.

Logic Analyzer	**16500B Software Version**	**16500C Software Version**	**Channel Count**	**State Speed**	**Timing Speed**	**Memory Depth**
16550A (two card)	v3.09	v1.03	204	100 MHz	250 MHz	4 k states
16554A (three card)	v3.13	v1.03	204	70 MHz	125 MHz	500 k states
16555A (three card)	v3.13	v1.03	204	110 MHz	250 MHz	1 M states
16555D (three card)	v3.13	v1.03	204	110 MHz	250 MHz	2 M states
16556A (three card)	v3.13	v1.03	204	100 MHz	200 MHz	1 M states
16556D (three card)	v3.13	v1.03	204	100 MHz	200 MHz	2 M states
16500B/C Mainframe	v3.13	v1.03				
Additional Equipment	**Software Version**					
16505A Prototype Analyzer	A.01.30					
HP E3493A Processor Probe	v2.15	Provides Run Control connection to the target system. Refer the *HP E3493A Processor Probe User's Guide* for operating instructions.				

The HP E2466C Preprocessor Interface consists of the configuration software, for configuring the logic analyzer and the HP 16505A Prototype Analyzer, and the preprocessor interface hardware, which connects to the target system and processes the signals.

For more information on the supported logic analyzers, the HP 16505A, or the microprocessor, refer to the appropriate reference manuals for those products.

Figure 1



HP E2466C Preprocessor Interface

In This Book

This book is the user's guide for the HP E2466C Preprocessor Interface. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into three chapters and one appendix:

Chapter 1 explains how to set up and configure the preprocessor interface and logic analyzer for state or timing analysis.

Chapter 2 provides reference information on the logic analyzer format specification and symbols configured by the preprocessor interface software, and information about the transaction tracker files. It also contains information about the inverse assembler.

Chapter 3 contains reference information on the preprocessor interface hardware, including the characteristics and signal mapping for the preprocessor interface.

Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manual for those products.

Contents

Figures

Tables

1

Setting Up the Preprocessor Interface

Setting Up the Preprocessor Interface

This chapter explains how to set up the HP E2466C Preprocessor Interface hardware and software, configure the preprocessor, and connect the preprocessor to supported logic analyzers. It also contains information on setting up the HP 16505A Prototype Analyzer for use with the HP E2466C Preprocessor Interface and using the HP E2467A APIC Bus Preprocessor Interface.

Before You Begin

This section lists the logic analyzers supported by the HP E2466C, and provides other information about the analyzers and the preprocessor.

Equipment Supplied

- The preprocessor interface circuit board.
- Cable, interposer, bottom clamp, and heat sink.
- The configuration files, for the logic analyzer and HP 16500B/C mainframe, on a 3.5-inch disk. There are also Demo files for all supported logic analyzers on the disk.
- Transaction tracker/inverse assembly software for the HP 16505A Prototype Analyzer on a 3.5-inch disk.
- This User's Guide.

Minimum Equipment Required

- The HP E2466C Preprocessor Interface, configuration files, and transaction tracker software.
- An HP 16505A Prototype Analyzer.
- A target system with the microprocessor circuit board removed from the S.E.C. cartridge. Detailed instructions for disassembling the S.E.C. cartridge can be found in Intel's *S.E.C. Cartridge Disassembly Application Note*.
- One of the logic analyzers listed in the table on page ii, in an HP 16500B/C Logic Analysis Mainframe.

For instruction disassembly, Branch Trace Messages must be enabled and instruction caches must be disabled. This requires a Pentium II processor run-control tool such as the HP E3493A, and a 30-pin debug port on the target system. The HP E3493A run-control tool requires firmware version v2.15 or higher for the Pentium II processor.

Additional Capabilities/Equipment Required

For APIC Bus analysis, the HP E2467A APIC Bus Preprocessor Interface can be used with the HP E2466C.

Additional configuration software for increased analysis of Pentium II processor target systems is available with the appropriate Intel non-disclosure forms. Contact your HP Sales Office for further information about the restricted version.

Setting Up the Preprocessor Interface Hardware

Setting up for the preprocessor interface hardware consists of the following major steps:

1. Turn off the logic analyzer and the target system.

CAUTION

To protect your equipment, remove the power from both the logic analyzer and the target system before you make or break connections. Because the logic analyzer supplies power to the preprocessor interface, the logic analyzer should always be powered up before the target system; when powering down, power down the target system first and then power down the logic analyzer.

2. Set the State/Timing Mode (Mode) switch and the Compacted/Expanded Clock Qualifier switch according to the type of analysis you wish to perform.
3. Disassemble the S.E.C. cartridge containing the microprocessor.
4. Install the preprocessor interface in the target system.
5. Connect the logic analyzer pods to the cable connectors of the preprocessor interface board.

To select the operating mode

Two switches on the preprocessor select the operating mode. The LEDs indicate the selected mode (see table 1). The HP 16505A Prototype Analyzer must also be updated to match the Mode (state or timing) selected by the switches.

The MODE switch selects either State or Timing mode. In State mode, the QUAL switch selects the clock qualifier to be either Compacted or Expanded. The QUAL switch has no effect in timing mode.

The Expanded clock qualifier acquires a state for every bus clock when there are transactions outstanding on the bus; no states are acquired when there are zero outstanding transactions.

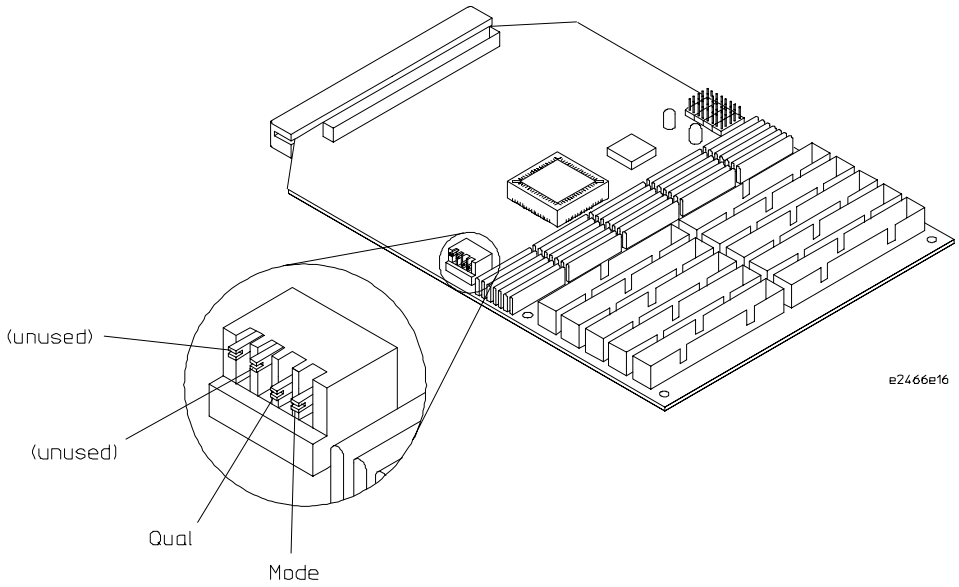
The Compacted clock qualifier maximizes the number of transactions captured and is generally preferred.

Refer to Chapter 3, section "Modes of Operation", for more details on the preprocessor operating modes and clock qualifiers.

Table 1. LED Indicators for Operating Mode

LEDs Lit	MODE Switch	QUAL Switch	Operating Mode/Clock Qualifier
Red only	Up	---	Timing
Red and Green	Down	Up	State with Expanded Clock Qualifier
Green only	Down	Down	State with Compacted Clock Qualifier

Figure 2



Switches for State/Timing Mode and Clock Qualifier

To disassemble the S.E.C. cartridge

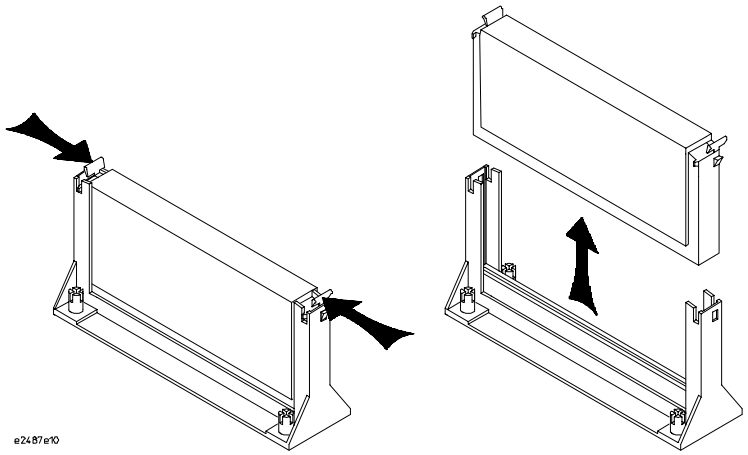
The S.E.C. cartridge consists of a thermal plate, skirt, cover, and microprocessor card. The thermal plate, skirt, and cover must be removed to access the processor card.

Detailed instructions for disassembling the S.E.C. cartridge can be obtained from Intel. The following procedures are only intended as an overview.

> Disassembling the S.E.C. cartridge voids the Intel warranty. Also, there is a high probability that the cover and thermal plate will be damaged during disassembly, and a small possibility that the microprocessor card will be damaged. The S.E.C. cartridge is not intended to be reassembled after disassembly.

1 Remove the S.E.C. cartridge from the target system by pushing in the two tabs on top of the cartridge, then pulling the cartridge up.

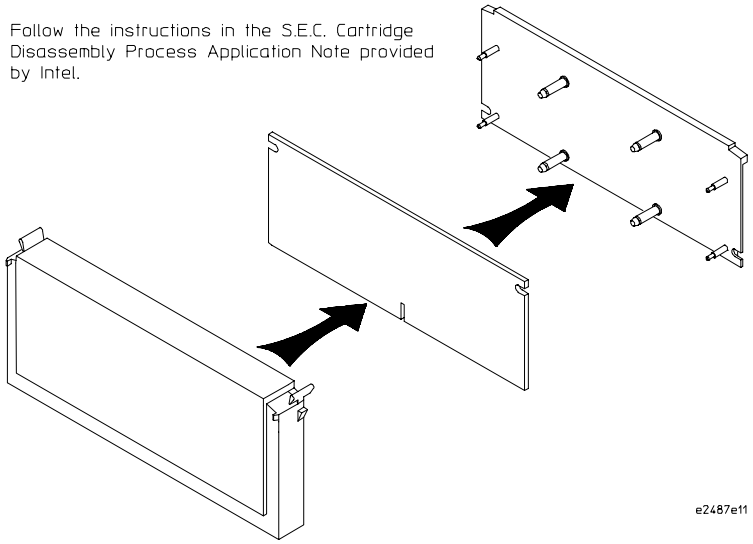
Figure 3



Removing the S.E.C. Cartridge

2 Using the instructions in the Intel *S.E.C. Cartridge Disassembly Application Note*, insert a 1/8" small flat blade screwdriver between the cover and the thermal plate, next to one of the four barbed posts located at each corner of the thermal plate. Twist the screwdriver until the barbed post pops free. Repeat this procedure for the other barbed post at the same end of the cartridge, then repeat for the other end of the cartridge.

Figure 4



Disassembling the S.E.C. Cartridge

3 Using the instructions in the Intel *S.E.C. Cartridge Disassembly Application Note*, use fine-tip round nose pliers to separate the tabs on the thermal plate away from the locator pins. Remove the spring retainer clips, then separate the thermal plate from the microprocessor circuit board.

To connect to the target system

The probe end of the preprocessor connects directly to the microprocessor on the target system.

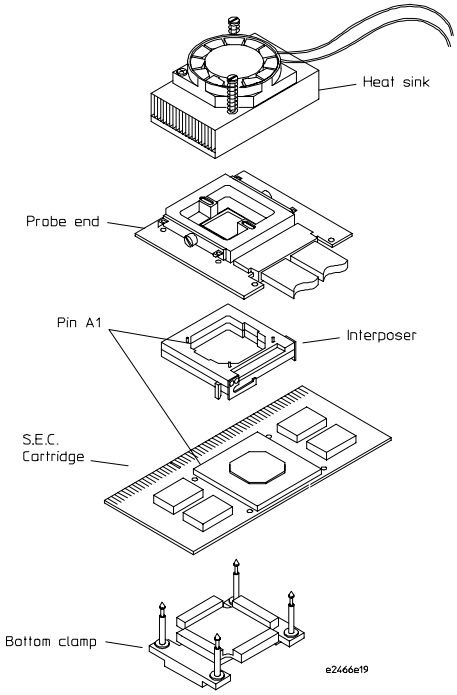
1 To prevent equipment damage, remove power from both the logic analyzer and the target system.

CAUTION

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin A1 on the preprocessor interposer and on the microprocessor before making any connection. Take care to align the preprocessor connector assembly with the pins on the microprocessor so that all pins make contact.

2 Install the interposer onto the microprocessor on the target system. The alignment tabs on the interposer aid in making proper alignment. Ensure that pin A1 is oriented correctly (see figure below).

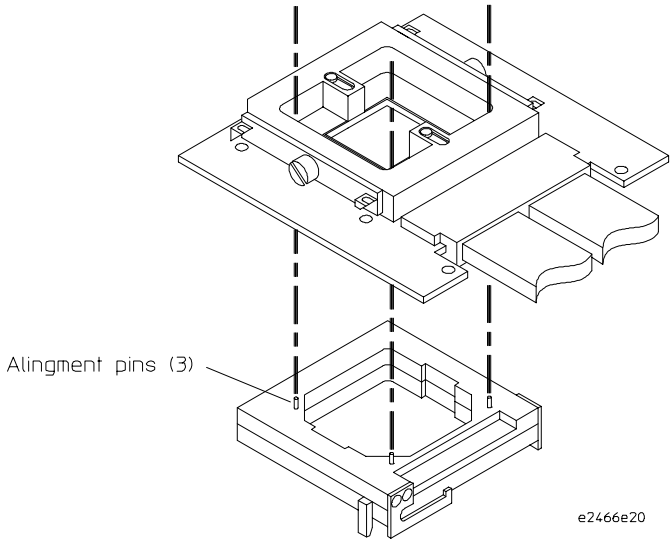
Figure 5



Probe Connection Overview

3 Place the probe end of the preprocessor interface onto the interposer using the three alignment pins as shown in the figure below.

Figure 6

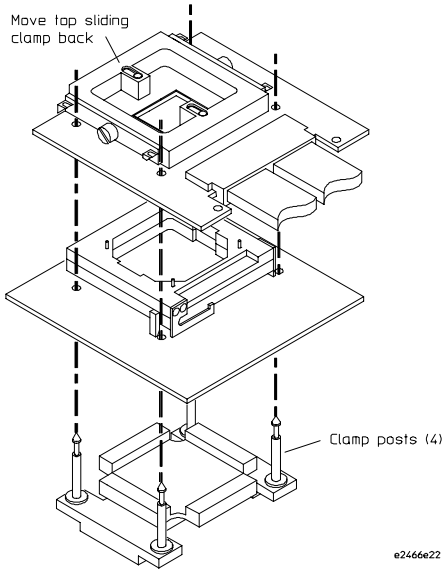


Aligning the Probe End

4 Loosen the screw on the underside of the bottom clamp.

5 Work the four clamp posts of the bottom clamp through holes in the target system PC board. Slide the clamp on the probe end of the PC board back, then work the four clamp posts on through the preprocessor PC board.

Figure 7



Securing the Preprocessor Connection

6 Move the top sliding clamp forward on the probe end until it holds the clamp posts of the bottom clamp.

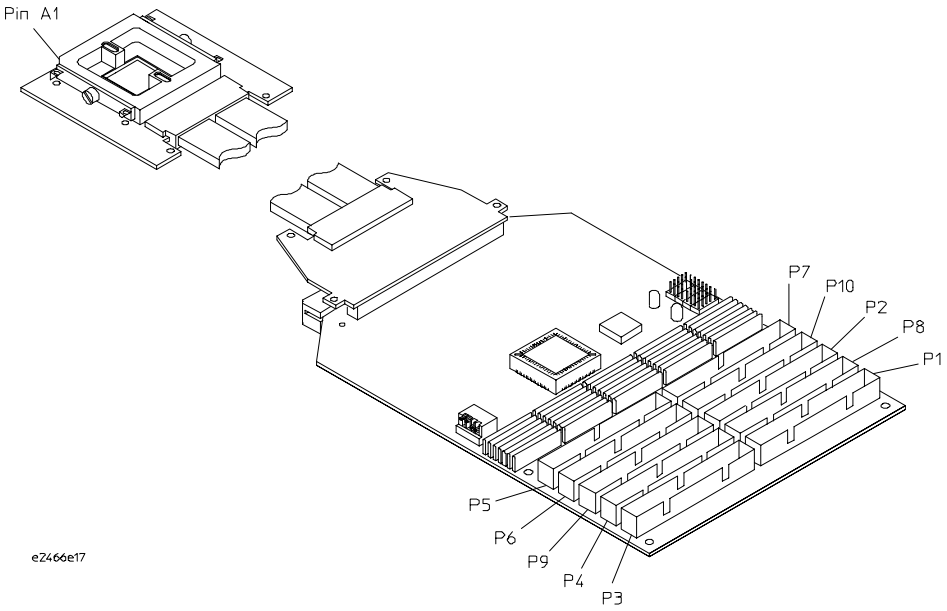
7 Tighten the screw on the underside of the bottom clamp until it is snug (80 inch-ounces of torque). If the screw is too loose, the preprocessor will not make good contact with the microprocessor pins. If the screw is too tight, it may damage the interface connector.

8 Insert the heat sink into the rectangular opening on top of the preprocessor interface. Select an orientation that does not interfere with the target system. Tighten the two screws until the heat sink is snug. Do not overtighten.

9 Connect the heat sink to a +12 Volt power source. The black wire is ground, and the yellow wire is positive. To protect your target system and the preprocessor interface, ensure the fan is running whenever the target system is powered.

10 Connect the preprocessor to the logic analyzer using the preprocessor connectors shown below and the logic analyzer pods shown on the following pages.

Figure 8

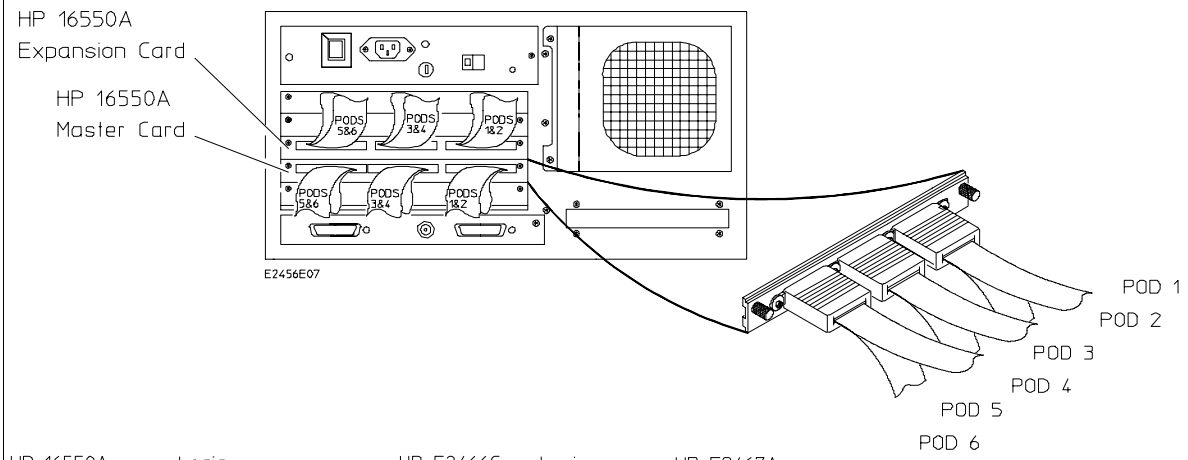


Preprocessor Connector Numbers and Pin A1 Location

CAUTION Support the HP E2466C PC board when connecting or disconnecting logic analyzer cables. This will help to prevent damage to the PC board and its components.

To connect to the HP 16550A two-card analyzer

Connect the logic analyzer pod cables to the preprocessor interface connectors according to this diagram.



HP 16550A Two-card Logic Analyzer	Logic Analyzer Pod	HP E2466C Pentium II Preprocessor	Logic Analyzer Label	HP E2467A APIC Bus Preprocessor
EXPANDER	Pod1	P5	DATA_B (L)	
EXPANDER	Pod2	P6	DATA_B (H)	
EXPANDER	Pod3	P7	ADDR (L)	
EXPANDER	Pod4	P8	ADDR (H)	
EXPANDER	Pod5	P9	ADDR_B (L)	
EXPANDER	Pod6	P10	ADDR_B (H)	
MASTER	Pod1			J1 Clk↑ DATA (L)
MASTER	Pod2			J2 DATA (H)
MASTER	Pod3	P1	STAT (L) Clk↑	
MASTER	Pod4	P2	STAT (H)	
MASTER	Pod5	P3	DATA (L)	
MASTER	Pod6	P4	DATA (H)	

e2467b02

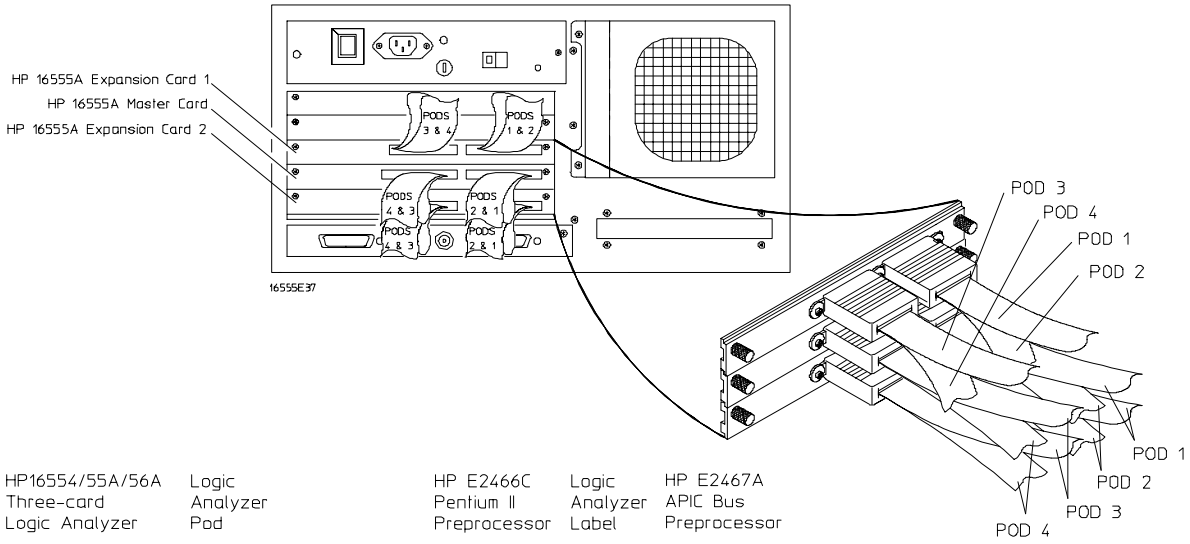
Configuration file

Use configuration file CP6C_2P for the two-card HP 16550A Logic Analyzer.

When using the HP E2467A APIC Bus Preprocessor Interface, Master Pod 1 and Master Pod 2 are connected for APIC analysis. In this case, use configuration file CP6C_2AP.

To connect to the HP 16554/55/56 analyzers

Connect the logic analyzer pod cables to the preprocessor interface connectors according to this diagram.



HP16554/55A/56A Three-card Logic Analyzer	Logic Analyzer Pod	HP E2466C Pentium II Preprocessor	Logic Analyzer Label	HP E2467A APIC Bus Preprocessor
EXPANDER 1	Pod1	P7	ADDR (L)	
EXPANDER 1	Pod2	P8	ADDR (H)	
EXPANDER 1	Pod3	P9	ADDR_B (L)	
EXPANDER 1	Pod4	P10	ADDR_B (H)	
MASTER	Pod1			J1 Clk↑ DATA (L)
MASTER	Pod2			J2 DATA (H)
MASTER	Pod3	P1	STAT (L) Clk↑	
MASTER	Pod4	P2	STAT (H)	
EXPANDER 2	Pod1	P3	DATA (L)	
EXPANDER 2	Pod2	P4	DATA (H)	
EXPANDER 2	Pod3	P5	DATA_B (L)	
EXPANDER 2	Pod4	P6	DATA_B (H)	

E2466B03

Configuration file

Use configuration file CP6C_1P for the HP 16554A/55A/56A Logic Analyzers.

When using the HP E2467A APIC Bus Preprocessor Interface, Master Pod 1 and Master Pod 2 are connected for APIC analysis. In this case, use configuration file CP6C_1AP.

To power up or power down

When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, and then the logic analyzer.

To protect the preprocessor interface when not in use

1 Cover the probe end of the preprocessor interface with a conductive padded wrapper.

The probe end of the preprocessor interface was covered at the time of shipment with a conductive padded wrapper. If this wrapper is not damaged, it may be reused repeatedly.

2 Store the preprocessor interface in an antistatic bag or container.

Electrostatic Discharge

Covering the probe end and properly storing the preprocessor interface also protects the active circuitry on the preprocessor interface from electrostatic discharge.

Setting Up the Preprocessor Interface Software

The preprocessor interface software consists of one HP 16500B/C Logic Analysis System disk and one HP 16505A Prototype Analyzer disk. The HP 16500B/C disk contains logic analyzer configuration files; the HP 16505A disk contains the transaction tracker and the inverse assembler.

To copy the HP 16500B/C logic analyzer files

1. **The first time you set up the preprocessor interface, make a duplicate copy of the master disk.**

   For information on duplicating disks, refer to the reference manual for your logic analyzer.

2. **Ensure that the HP 16500B/C mainframe and the logic analyzer module have the required software version of the operating system.**

   The version requirements are listed on page ii.

3. **Insert the "HP 16500B/C Logic Analyzer Configs" flexible disk in the disk drive of the HP 16500B/C.**
4. **Select the "System, Hard Disk" menu.**
5. **Create a directory on the logic analyzer using the command sequence "Make Directory, new directory name: <name>, Execute".**
6. **Select the "System, Flexible Disk" menu. Copy all files to the directory on the hard disk using the command sequence "Copy, file: *, to:\<name> on: Hard Disk, Execute".**

   The logic analyzer is configured through the HP 16505A, using the files you have just copied onto the logic analyzer hard drive.

To load the HP 16505A Prototype Analyzer files

The HP 16505A Prototype Analyzer is required for transaction tracking and inverse assembly. To set up the prototype analyzer:

1. If you have not already done so, copy the logic analyzer files as described in the previous section.

   The HP 16500B/C files must be copied to the logic analyzer hard drive first for the HP 16505A to access them.

2. Connect the HP 16505A to the HP 16500B/C. Power up the HP 16500B/C first, then power up the HP 16505A.

   For information on connecting the HP 16505A, refer to the *HP 16505A Installation Guide*.

3. Ensure that the HP 16505A has software version A.01.30 or greater.

   You may check the HP 16505A system version from a running session. In the Main window, click Help, then click "On Version...".

4. Install the HP 16505A software for the Pentium II processor.

   Place the "HP 16505A Prototype Analyzer Disk" flexible disk in the disk drive of the HP 16505A. In the Session Manager window, select the **`Update`** button. The window should display

   Filegroup: pp_pentium2
   Version: A.01.30.

   Click on Update/Install and respond to the question by clicking on OK. Wait for the Information dialog to confirm a successful installation. Click on OK to acknowledge, and Close the Update/Install window.

5. Load the logic analyzer configuration file.

   Start a session from the Session Manager window. When the main HP 16505A window opens, click on File in the top menu bar to get a pull-down menu, then click on "Load 16500 Files...". Change to the appropriate directory and load the appropriate file, either CP6C_1P or CP6C_2P (for Pentium II processor only analysis) or CP6C_1AP or CP6C_2AP (for Pentium II processor and HP E2467A APIC Bus analysis). Next, drag and drop the "Pentium II" Instrument icon into the workspace area. Next, drag and drop a Listing Display on the "Pentium II" Instrument icon in the workspace. Double click on the Listing icon to open the Listing window and verify that the label "Pentium II Inverse Assembly" appears.

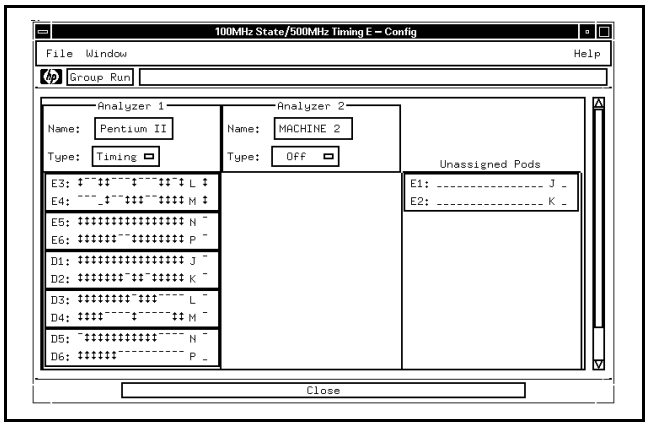
To set up the preprocessor interface for timing

The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1. Configure the HP E2466C for timing analysis by setting the MODE switch to the "Up" position. Only the Red LED should be lit.
2. Select the "Pentium II" icon on the HP 16505A, and open the Config menu of the logic analyzer.
3. Select the Type field for the analyzer and select Timing.

   The following figure shows the HP 16505A Config Menu display for the HP 16550A logic analyzer:

Figure 9



Configuration Menu with Timing Mode

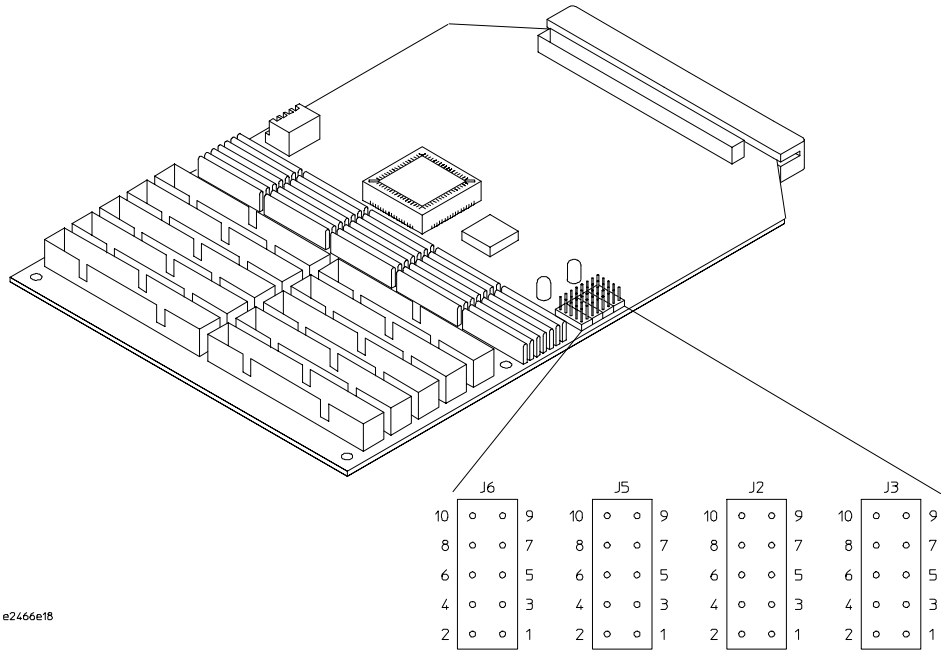
To connect to the APIC and JTAG signals

The APIC and JTAG signals are routed to headers J2 and J3, located next to the green LED. These signals can be probed using the GP [General Purpose] probes that are shipped with your logic analyzer. Figure 10 shows the location of the headers. Table 2 shows the signals that are located on the pins of each header. These signals, with the exception of "lreset", are buffered versions of the Pentium II processor bus signals; they are not latched by the bus clock. The special signal "lreset" is an inverted version of the P6 RESET# signal and is latched by the bus clock.

Do not attempt to use the JTAG header as a run-control interface. This header is only capable of monitoring JTAG activity.

The APIC signals can be connected to the HP E2467A APIC Bus Preprocessor Interface. Connectors J5 and J6 on the preprocessor PC board are reserved.

Figure 10



Pin locations for APIC and JTAG signals

Table 2. Pin locations for APIC and JTAG signals (J5 and J6 are reserved)

J2 (APIC)				J3 (JTAG)			
Pin #	**Signal**	**Pin #**	**Signal**	**Pin #**	**Signal**	**Pin #**	**Signal**
10	n/c	9	n/c	10	GND	9	TRST#
8	n/c	7	Ireset	8	GND	7	TDO
6	GND	5	PICD1#	6	GND	5	TDI
4	GND	3	PICD0#	4	GND	3	TMS
2	GND	1	PICCLK	2	GND	1	TCK

2

Analyzing the Pentium II Processor

Analyzing the Intel Pentium II Processor

This chapter describes how to display configuration information and preprocessor interface data, gives label and symbol encodings for the status field, and provides information about the transaction tracker and the inverse assembler, as displayed on the HP 16505A.

Displaying Information

This section describes how to display logic analyzer configuration information, state and timing data captured by the preprocessor interface, and symbol information that has been set up by the preprocessor interface configuration software.

To set up the HP 16505A workspace

To set up the HP 16505A workspace, drag and drop the "Pentium II" Instrument icon into the workspace area. Next, drag and drop a Listing Display on the "Pentium II" Instrument icon in the workspace. Double click on the Listing icon to open the Listing window and verify that the label "Pentium II Inverse Assembly" appears.

To display the format specification

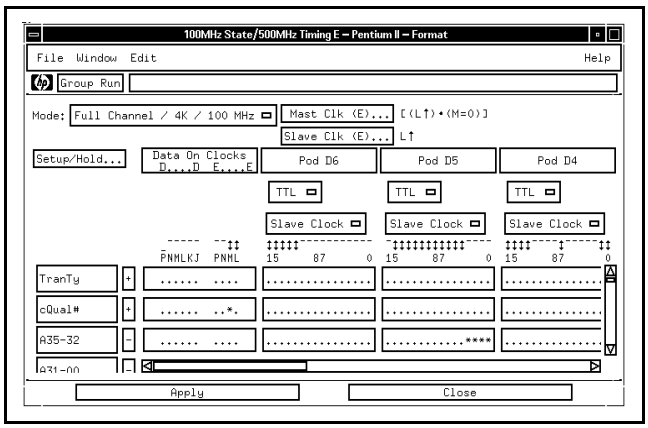
- **Using the mouse, right-click and hold on the instrument icon for the logic analyzer. In the pop-up menu, slide down to "Format..." then release the mouse button.**

  The HP E2466C configuration files contain predefined format specifications. These format specifications include all labels for monitoring the microprocessor bus.

  Chapter 3 of this guide contains a table that lists the signals for the Pentium II processor and on which pod and probe line the signal comes to the logic analyzer. Refer to this table and to the logic analyzer connection information for your analyzer in chapter 1 to determine where the processor signals should be on the format specification screen.

The format specification display shown in the following figure is from the HP 16550A logic analyzer. Additional labels and pod assignments are listed off the screen. Scroll vertically to view additional signals. Scroll horizontally to view other pod-bit assignments. There may be some slight differences in the display for your particular analyzer.

Figure 11



Logic Analyzer Format Specification

To display the configuration symbols

- **Using the mouse, right-click and hold on the instrument icon for the logic analyzer. In the pop-up menu, slide down to "Symbol..." then release the mouse button. Choose a label name from the "Label" list, then select "User Defined Symbols...." The logic analyzer will display the symbols associated with the label.**

  The HP E2466C configuration software sets up symbol tables. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels simplify triggering on specific Pentium II processor cycles. The label base in the symbols menu is set to hexadecimal to conserve display space.

  All Pentium II processor signals are routed to the logic analyzer probe headers or to extra headers. Labels that contain all lower case letters are signals that are created by the preprocessor hardware; these signals are described more fully in chapter 3, "Modes of Operation". Labels that begin with an uppercase letter and have lower case letters within them are signals that combine preprocessor generated signals and Pentium II processor signals.

The first of the following tables describes the Pentium II processor signals that are captured by the preprocessor. The second table lists the label and symbol encodings defined by the logic analyzer configuration software.

Note

Under the heading "Polarity", negative means that the logic analyzer inverts the signal. Positive means that the logic analyzer does not invert the signal.

Table 3. Signal/Label List

Label Name	Polarity	Number of bits	Description
A20M#	positive	1	Address bit 20 Mask signal
A35-32	negative	4	Address bus bits 35:32
A31-00	negative	32	Address bus bits 31:00
ADS#	positive	1	Address Strobe
AERR#	positive	1	Address Parity Error signal
AP#	positive	2	Address Parity signals
BCLK	positive	1	Bus Clock signal
BERR#	positive	1	Bus Error signal
BINIT#	positive	1	Bus Initialization signal
BNR#	positive	1	Block Next Request signal
BP3#	positive	1	Breakpoint signal
BP2#	positive	1	Breakpoint signal
BPM1#	positive	1	Breakpoint and Performance Monitor signal
BPM0#	positive	1	Breakpoint and Performance Monitor signal
BPRI#	positive	1	Priority Agent Bus Request signal
BR#	positive	4	Symmetric Agent Bus request signals
D63-32	negative	32	Data bus bits 63:32
D31-00	negative	32	Data bus bits 31:00
DBSY#	positive	1	Data Bus Busy signal
DEFER#	positive	1	Defer signal
DEP#	positive	8	Data bus ECC/Parity signals
DRDY#	positive	1	Data Ready signal
FERR#	positive	1	Floating-point Error signal
FLUSH#	positive	1	Flush signal

Label Name	Polarity	Number of bits	Description
FRCERR	positive	1	Functional Redundancy Check Error signal
HIT#	positive	1	Snoop Hit signal
HITM#	positive	1	Snoop Hit Modified signal
IERR#	positive	1	Internal Error signal
IGNNE#	positive	1	Ignore Numeric Error signal
INIT#	positive	1	Initialization signal
INTR	positive	1	Interrupt Request signal
LINT	positive	2	Local Interrupt signals
LOCK#	positive	1	Bus Lock signal
NMI	positive	1	Non-maskable Interrupt signal
PRDY#	positive	1	Probe Ready signal
PREQ#	positive	1	Probe Request signal
RESET#	positive	1	Reset signal
RP#	positive	1	Request Parity signal
RS#	positive	3	Response Status
RSP#	positive	1	Response Parity signal
SMI#	positive	1	System Management Interrupt signal
STPCK#	positive	1	Stop Clock signal
TRDY#	positive	1	Target Ready signal

The following table lists the transaction type symbol encodings defined by the logic analyzer configuration software for the TranTy label.

Table 4. Pentium II Processor Transaction Type Symbols

Signal	Symbol
TranTy	"Branch Trace" "Code Read " "Data Read " "Defer Reply " "Int Ack/Spcl" "Invalidate " "I/O Read " "I/O Write " "Mem Write " "RSVD_1 " "RSVD_2 " "RSVD_3 " "RSVD_4 " "Writeback " "--- "

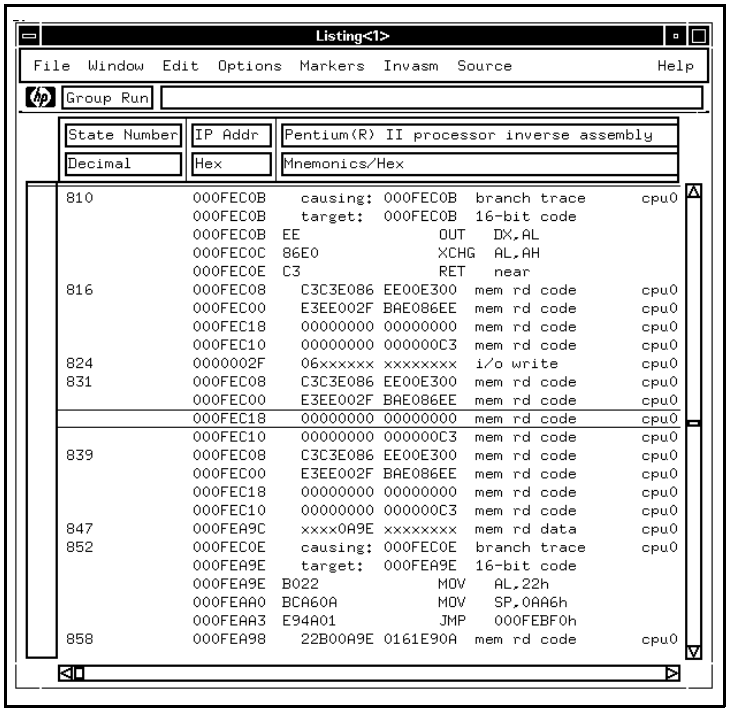
To display captured state information

The captured information is displayed in the Listing display.

- **Open the Listing display for your logic analyzer.**
  If your trace listing doesn't otherwise appear to be correct (capturing the same RAM address twice, for example), make sure the preprocessor interface hardware is configured for state analysis. See Chapter 1 to review the hardware configuration, correct it if needed, and then run the trace again.

Figure 12 shows the Listing display for the HP 16550A logic analyzer.

Figure 12

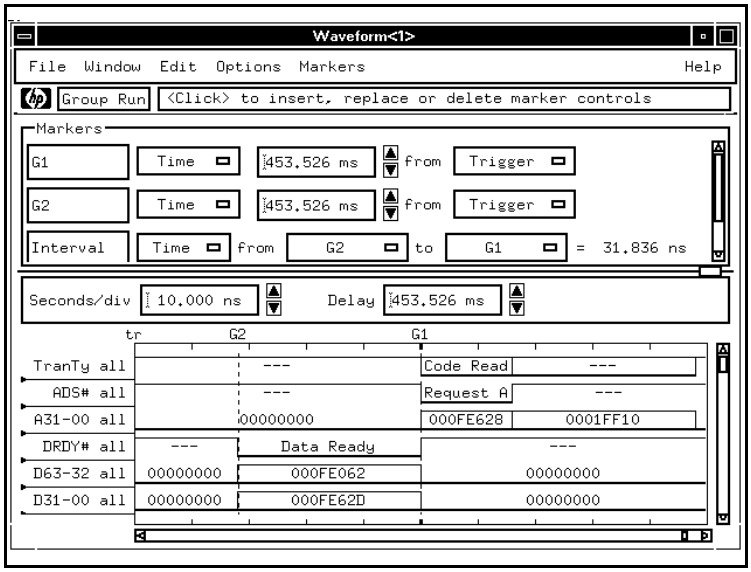


Logic Analyzer Listing Display

To display captured timing data

- Open the Waveform display for your logic analyzer.
  The following figure shows the Waveform display for the HP 16550A logic analyzer:

Figure 13



Logic Analyzer Waveform Display

Using the Transaction Tracker

This section discusses the general output format of the transaction tracker, and any processor-specific information you will need.

The transaction tracker supports many filter options based on type of states (start of a transaction, part of some transaction), transaction types, and transaction-agent ownership. The next few paragraphs describe the general output format of the transaction tracker.

Data Format

The transaction tracker processes the captured data in a transaction-based format.

Numeric Format

For the data phase display, the numeric output from the transaction tracker is in hexadecimal format. All other numbers are in decimal format.

Filter options

The transaction tracker supports many filter options based on types of states (start of a transaction, part of some transaction), transaction types, and transaction ownership. The following is a list of the filter options available.

Filterable State	**Options**
Show Phases	
Request Phase A:	Show/Suppress
All Phases:	Show/Suppress
Agents	
CPU 0:	Show/Suppress
CPU 1:	Show/Suppress
CPU 2:	Show/Suppress
CPU 3:	Show/Suppress
Priority:	Show/Suppress

Filterable State	Options
Show Transactions:	
Code Reads:	Show/Suppress
Memory Data Reads:	Show/Suppress
Mem Read & Invalidate:	Show/Suppress
Memory Writes:	Show/Suppress
Memory Writebacks:	Show/Suppress
I/O Reads:	Show/Suppress
I/O Writes:	Show/Suppress
Deferred Replies:	Show/Suppress
Interrupt Acknowledges:	Show/Suppress
Special Transactions:	Show/Suppress
Branch Trace Messages:	Show/Suppress

Show/Suppress

The Suppress/Show settings determine whether the various microprocessor operations are shown or suppressed on the logic analyzer display. The preceding section shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function gives you a better analysis display in two ways. First, unneeded information can be filtered out of the display. Second, particular operations can be isolated by suppressing all other operations. For example, I/O accesses can be shown, with all other operations suppressed, allowing quick analysis of I/O accesses.

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

Transaction tracker messages

Any of the following messages may appear during analysis of your target software. Included with each message is a brief explanation.

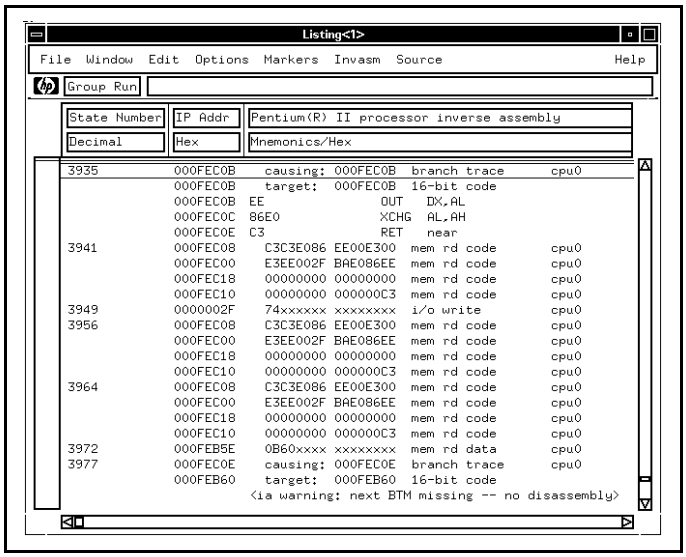
Errors and warnings

The HP E2466C software contains error messages and warnings for both the transaction tracker and the inverse assembler. For a list and description of the messages, refer to Appendix A.

Reaching boundaries

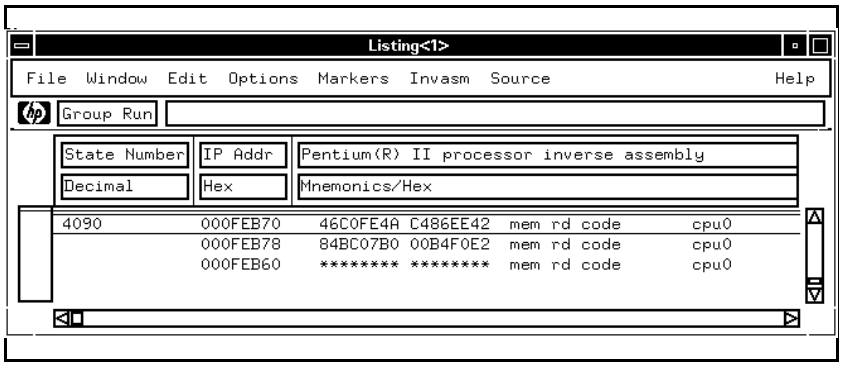
If the transaction tracker internal search limit (8192 states per transaction) is exceeded, or if part of a transaction is not acquired at the end of the analyzer acquisition memory, error messages may be displayed. Figure 14 shows a warning message. Figure 15 shows the end of a boundary.

Figure 14



Listing Display with Boundary Error Message

Figure 15



Listing Menu Showing End of Boundary

Protocol Violations

The transaction tracker displays a bus protocol violation when the maximum allowable outstanding transactions have been exceeded.

Protocol violations are followed with line:

"*** protocol violation detected ***"

> The transaction tracker does not attempt to do a complete job of detecting protocol violations. Undetected protocol violations may cause the transaction tracker to display incorrect results.

Using the Inverse Assembler

In addition to basic transaction tracking, the HP 16505A can display an accurate instruction execution trace of Pentium II processor target systems containing up to four processors. Instruction disassembly supports Intel's MMX technology. Disassembly requires the use of a separate run-control tool such as the HP E3493A to disable all CPU caches and enable Branch Trace Message transactions.

Operating modes are determined by a combination of preprocessor interface hardware switch settings and options selected in the HP 16505A Listing window under the "Invasm - Filter..." and "Invasm - Preferences..." menu pull-downs. The Filter dialog allows the user to show, suppress, or change the color of an entire acquisition state, whereas the Preferences dialog controls the display format for a state which is shown.

> Disassembly is only possible when "Display Disassembly" is selected in the Preferences dialog and "Branch Trace Messages" are selected in the Filter dialog. Additionally, a run-control tool should be used to enable Branch Trace Messages and disable the instruction caches for all processors.

Hardware switches

The inverse assembler software requires that switches on the preprocessor interface hardware be set to one of the modes listed below.

- State Mode with Expanded Clock Qualifier
- State Mode with Compacted Clock Qualifier

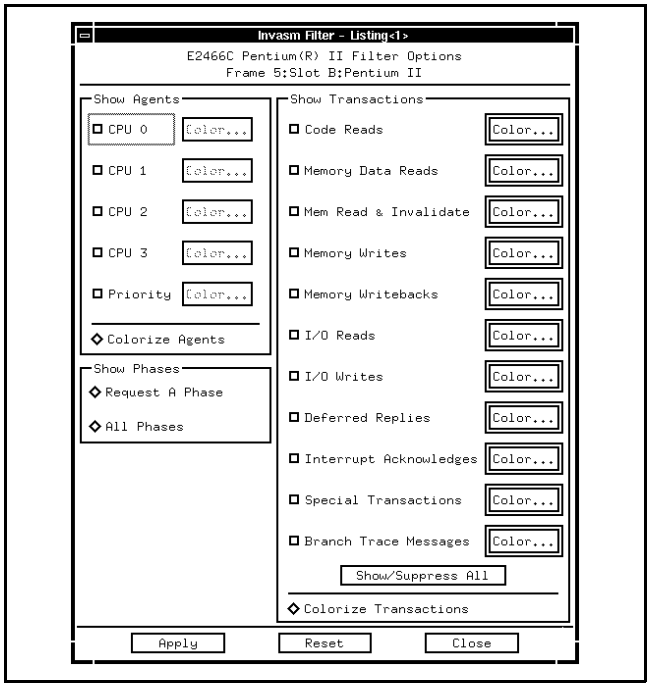
Refer to Figure 2 in Chapter 1 for correct switch positions. If the switches are mistakenly set to Timing mode, the "inverse assembly" column in the Listing window displays an error message.

See Appendix A for a complete list of error messages.

Pentium II filter dialog

Filter options are accessed from the Listing menu bar by clicking on Invasm and selecting Filter. The Filter dialog provides the ability to display only information for particular bus agents and/or transaction types. Colorization can be used to identify either transactions or processors. Show Phases allows you to show only the Request A Phase, which contains a summary of the entire transaction, or All Phases, which includes all captured states pertaining to each transaction. The figure below shows a sample Filter dialog.

Figure 16



HP 16505A Pentium II Filter Dialog

Pentium II preferences dialog

Preferences options are accessed from the Listing menu bar by clicking on Invasm and selecting Preferences. The Preferences dialog controls the level of detail for states shown. Figure 17 shows the Preferences dialog.

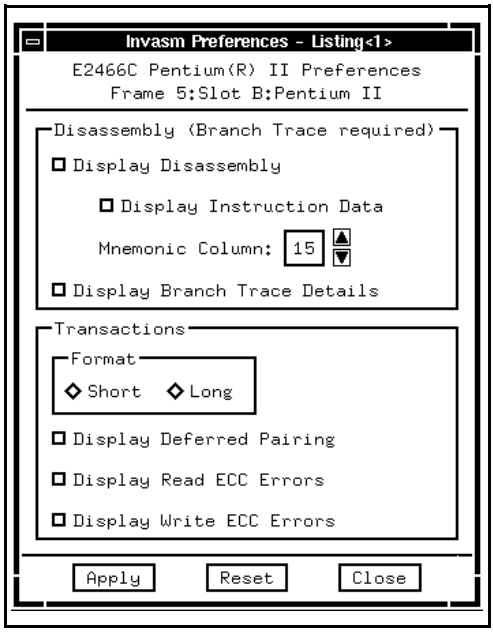
Disassembly

When "Display Disassembly" is selected, a block of instructions appears in the Listing window under each Branch Trace Message transaction or Memory Code Read from the reset vector (the instruction cache(s) must be disabled). "Display Instruction Data" turns on/off the display of data bytes corresponding to each instruction. "Display Branch Trace Details" shows the causing and target linear addresses contained in each Branch Trace Message transaction.

Transactions

The transaction Format can be set to "Short" to display one line per transaction data chunk (DRDY# asserted state), or "Long" for more extensive information about the phases. "Display Deferred Pairing" consolidates the deferred reply transaction information directly beneath the original deferred transaction. "Display Read/Write ECC Errors" examines the D[63:00]# and DEP[7:0]# signals during DRDY# asserted states and displays detected errors not on the data phase, but on the Request phase which started the transaction. Bad bits are identified for single-bit correctable errors. These ECC options should only be selected when data bus error-checking is enabled on the target system. While CPU agents usually drive DEP[7:0]#, non-CPU agents may or may not, so exercise judgement when turning on "Display Read ECC Errors".

Figure 17



HP 16505A Pentium II Preferences Dialog

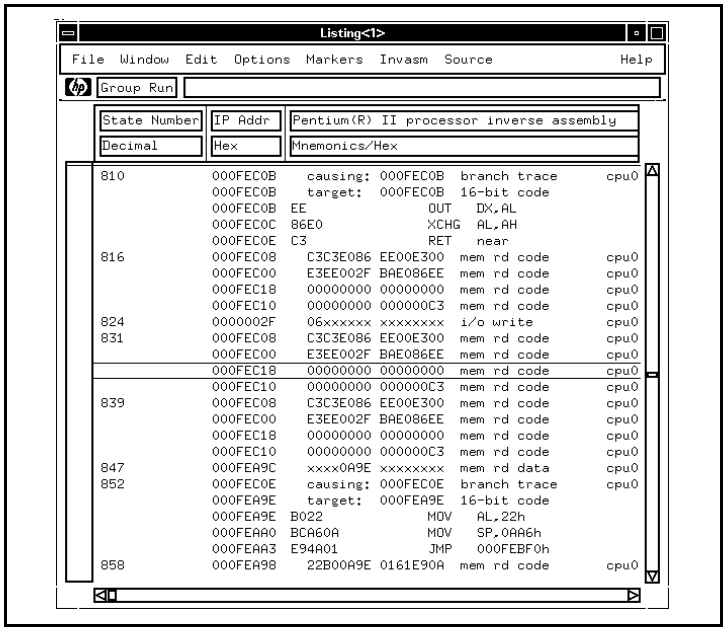
Analysis techniques

Suggested Settings

For software analysis, the settings below give a high-level view of the captured data. Remember to disable the processor instruction caches and enable Branch Trace Messages in order to get disassembly.

Switches:	State Mode with Compacted Clock Qualifier.	
Filter:	Show Agents	-- Show All
	Show Transactions	-- Show All except Code Reads
	Show Phases	-- Request A Phase
Preferences:	Display Disassembly	-- ON
	Display Branch Trace Details	-- OFF
	Transaction Format	-- SHORT
	Display Deferred Pairing	-- ON
	Display Read ECC Errors	-- OFF
	Display Write ECC Errors	-- ON

Figure 18



HP 16505A Listing window for Software Analysis

For hardware analysis, the State and Timing Waveform displays provide the most relevant details. If these displays to not provide the level of detail required for your analysis needs, you might need the restricted version of the HP E2466C. Contact your HP Sales Office for information on obtaining the appropriate Intel non-disclosure forms for the restricted version.

Disassembler Behavior

To display instruction disassembly, use a Pentium II processor run-control tool such as the HP E3493A to enable Branch Trace Messages and disable the processor instruction caches. Show "Branch Trace Messages" in the Filter dialog, and select "Display Disassembly" in the Preferences dialog.

When a processor executes a branching instruction, the prefetch queues are flushed, a Branch Trace Message (BTM) appears on the bus, and the processor begins fetching code at the branch target address. The disassembly software finds matching code reads between the current BTM and the next matching BTM, reorders any out-of-order bursts, then disassembles the code read data. In searching for code reads, any fetches which are deferred are automatically paired with their corresponding deferred replies to ensure that all code read data is found. This pairing is not affected by the "Display Deferred Pairing" setting in the Preferences dialog.

Physical vs. Linear Addresses

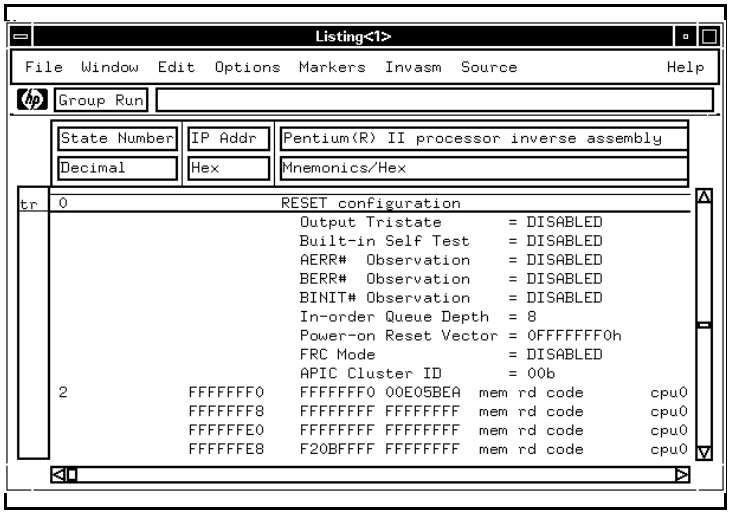
Branch Trace Messages give linear causing and target addresses. The addresses displayed for Memory Code Read transactions are physical. For real-mode programs, this is not an issue since linear and physical addresses are equivalent. For protected-mode programs with paging enabled, the address bits higher than A[11] will usually be different. Linear addresses for disassembled instructions are shown in the "IP Addr" column of the Listing window.

The following table describes the reset configuration information that is displayed at reset.

Table 5. Reset Configuration

Signal at Reset	Configuration (asserted/deasserted)
FLUSH#	Output Tristate Enabled/Disabled
INIT#	Built-in Self Test Enabled/Disabled
A8#	AERR# Observation Policy Enabled/Disabled
A9#	BERR# Observation Policy Enabled/Disabled
A10#	BINIT# Observation Policy Enabled/Disabled
A7#	In-order Queue depth = 1/8
A6#	Power-on Reset Vector = 000FFFF0 or FFFFFFF0 hex
A5#	FRC Mode Enabled/Disabled
A[12:11]#	APIC Cluster ID (00, 01, 10, 11)

Figure 19



Reset Configuration

Triggering Hints

Storage Qualification

Any use of storage qualification in the trigger sequence will result in error messages in the inverse assembly column in the Listing. The preprocessor interface communicates its switch settings and dynamic AERR/BINIT observation policies to the logic analyzer via a repeating serial frame on a preprocessor-generated signal. Storage qualification interrupts this serial frame, resulting in transaction tracker/disassembler errors.

Triggering on address and transaction type

To trigger on a specific address and transaction type, use the A35-32, A31-00, and TranTy labels, together with the TranTy label symbols. The symbols identify each transaction type uniquely, except for Interrupt Acknowledge and Special Transactions, which are combined into one symbol.

Triggering on data and transaction type

There is no guaranteed method of triggering on a particular transaction type or address ANDed with a particular data value in a target system with overlapping transactions. Although the Listing displays a transaction type and 8-byte data value on the same line when Transaction Display Mode is set to Short, this alignment is the result of post-processing and cannot be used for triggering. The preprocessor interface hardware captures this information on different states. A trigger specification could be defined to find a certain transaction type in the Request A phase, then trigger on a data value qualified by DRDY# asserted; however, by the time the data pattern is found, it could belong to a different transaction.

3

Preprocessor Interface Hardware Reference

Preprocessor Interface Hardware Reference

This chapter contains reference information on the HP E2466C hardware including the characteristics and signal mapping for the preprocessor interface. This chapter also includes a brief theory of operation, circuit board dimensions, and information on servicing the preprocessor interface.

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the preprocessor interface.

Table 6. Operating Characteristics

Microprocessor Compatibility	Intel Pentium II microprocessor
Microprocessor Package	S.E.C. Cartridge
Clock Frequency	66 MHz maximum for external BCLK
Target Signal Amplitude	800 mV p-p minimum for all GTL+ signals
Logic Analyzers Supported	16550A (two-card module) 16554A (three-card module) 16555A/D (three-card module) 16556A/D (three-card module)
Accessories Required	None.
Timing Analysis	3 nS channel-to-channel skew (typical)
Power Requirements	Supplied by the logic analyzer.
Probes Required	Ten logic analyzer pods are required for transaction tracking.
Signal Line Loading	Varies (see description on page 3-5).

Table 6. Operating Characteristics

Environmental Temperature	Operating	0 to 55 degrees C (+32 to +131 degrees F)
	Nonoperating	-40 to +75 degrees C (-40 to +167 degrees F)
Altitude	Operating	4,600 m (15,000 ft)
	Nonoperating	15,300 m (50,000 ft)
Humidity	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Table 7. Product Regulations

Safety	IEC 348/EN 61010-1 : 1993 UL 1244 CSA Standard C22.2 No.231 (Series M-89)

Signal line loading

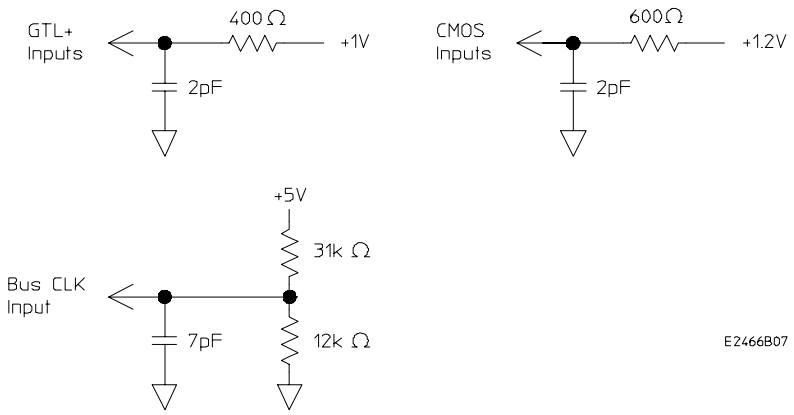
The figure below shows the equivalent loads placed on the microprocessor bus by the preprocessor interface. The loading is not affected by the preprocessor operating mode.

The CMOS model applies to the following list of signals:

Table 8. CMOS Inputs

3.3V Tolerant	APIC Group	JTAG Group
A20M#	PICCLK	TCLK
FERR#	PICD1#	TRST#
FLUSH#	PICD0#	TMS
IERR#		TDI
IGNNE#		TDO
INIT#		
LINT0/INTR		
LINT1/NMI		
PREQ#		
SMI#		
STPCLK#		

Figure 20



Signal Line Loading

Modes of operation

The preprocessor interface can operate in State mode or Timing mode. In State mode, the logic analyzer master clock is always qualified with the "cqual#" signal from the preprocessor. This clock qualifier is set to either Compacted or Expanded. By eliminating idle clocks, the Compacted qualifier can potentially capture many more transactions than the Expanded qualifier. Refer to chapter 1 for information on configuring the preprocessor interface and logic analyzer for the desired mode of operation.

State Mode Operation

State mode uses the BCLK rising edge to capture the signals from the Pentium II processor bus and to clock the logic analyzer. A PLD in the preprocessor generates additional information about each clock. The PLD information along with the bus signals are sent to the logic analyzer and used by the transaction tracker and inverse assembler to produce the transaction display (see Figure 21, Block Diagram).

Pentium II processor signals require a three-clock latency to move the information from the processor pins to the logic analyzer memory (except for the three bus signals on connector P1, which only require two clocks). The first clock is used to capture all of the bus signals in latches on the preprocessor. The second clock is used to move the bus signals from the preprocessor latches into the logic analyzer slave register. The slave latches exists within the logic analyzer, not in the preprocessor. Also, on the second clock, the PLD uses the signals that were captured on the first clock to generate additional information. The third clock is used by the logic analyzer to trigger on and/or store the data and the PLD information.

> The preprocessor interface captures but does not display the REQ[4:0]# bus signal group.

State Mode Clocking

To utilize the logic analyzer slave latches, the logic analyzer is configured to operate in "master/slave" mode. The logic analyzer uses the BCLK [L↑] to capture all pod data, except the pod connected to preprocessor connector P1, in the slave register. Connector P1 carries the PLD signals and is

assigned to the master clock [(L↑) • (M = 0)] which clocks the PLD information and the slave register outputs into the logic analyzer. The "cqual#" (M = 0) signal from the PLD is used to qualify the master clock to eliminate the collection of unnecessary data.

> The logic analyzer master clock must always include the M=0 qualifier for the transaction tracker to operate properly.

State Mode Buffered Signals

In state mode, most of the signals are latched by the bus clock before being routed to the logic analyzer. The following signals, however, are always buffered instead of latched:

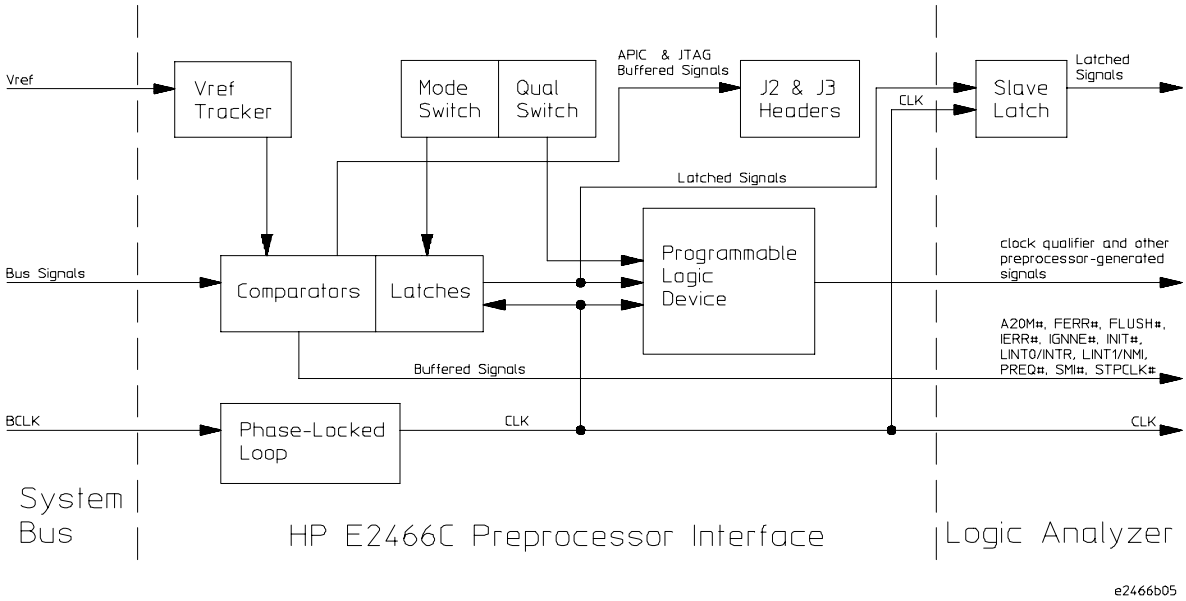
APIC & JTAG groups
A20M#
FERR#
FLUSH#
IERR#
IGNNE#
INIT#
LINT0/INTR
LINT1/NMI
PREQ#
SMI#
STPCLK#

Timing Mode Operation

The HP E2466C acts as a buffer in timing mode. The buffer in the preprocessor passes each Pentium II processor signal to the logic analyzer regardless of the state of BCLK. The slave latch within the logic analyzer is also bypassed and the PLD does not generate supplemental information. The transaction tracker will not operate when the preprocessor is in timing mode.

HP E2466C Block Diagram

Figure 21



HP E2466C Block Diagram

Signal-to-Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2466C Preprocessor Interface. Since the pods on the logic analyzers are numbered differently than the preprocessor connectors, refer to the tables in chapter 1 to correlate the pod numbers.

The signal list table column descriptions are as follows:

PREPROCESSOR CONNECTOR	NAME	The preprocessor connector that carries the signal.
	PIN	The pin within the preprocessor connector that carries the signal.
	BIT	The bit position of the signal within the preprocessor connector.
CPU	SIGNAL	The microprocessor signal name.
ANALYZER	LABEL(S)	The analyzer label assigned to the signal. Lower case letters indicate a preprocessor generated signal.

Table 9. Pentium II Processor Signal List

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	**PIN**	**BIT**	**SIGNAL**	**LABEL**
P1	3	CLK1	BCLK	BCLK
P1	7	D15	LINT0/INTR	LINT0 **
P1	9	D14	FLUSH#	FLUSH#
P1	11	D13	INIT#	INIT#
P1	13	D12	*	
P1	15	D11	*	
P1	17	D10	*	
P1	19	D9	*	
P1	21	D8	*	
P1	23	D7	*	
P1	25	D6	*	
P1	27	D5	*	
P1	29	D4	*	
P1	31	D3	*	
P1	33	D2	*	
P1	35	D1	*	
P1	37	D0	*	

* These signals are generated by the preprocessor interface.
** These signals are buffered (not latched) in State mode.

Table 9. Pentium II Processor Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL
P2	3	CLK1	*	cqual#
P2	7	D15	BR3#	BR#
P2	9	D14	BR2#	BR#
P2	11	D13	BR1#	BR#
P2	13	D12	BR0#	BR#
P2	15	D11	BPRI#	BPRI#
P2	17	D10	BNR#	BNR#
P2	19	D9	LOCK#	LOCK#
P2	21	D8	ADS#	ADS#
P2	23	D7	*	
P2	25	D6	*	
P2	27	D5	*	
P2	29	D4	*	
P2	31	D3	*	
P2	33	D2	HIT#	HIT#
P2	35	D1	HITM#	HITM#
P2	37	D0	DEFER#	DEFER#

* These signals are generated by the preprocessor interface.

Table 9. Pentium II Processor Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL
P3	3	CLK1	IGNNE#	IGNNE#
P3	7	D15	D15#	D31-00
P3	9	D14	D14#	D31-00
P3	11	D13	D13#	D31-00
P3	13	D12	D12#	D31-00
P3	15	D11	D11#	D31-00
P3	17	D10	D10#	D31-00
P3	19	D9	D9#	D31-00
P3	21	D8	D8#	D31-00
P3	23	D7	D7#	D31-00
P3	25	D6	D6#	D31-00
P3	27	D5	D5#	D31-00
P3	29	D4	D4#	D31-00
P3	31	D3	D3#	D31-00
P3	33	D2	D2#	D31-00
P3	35	D1	D1#	D31-00
P3	37	D0	D0#	D31-00

Table 9. Pentium II Processor Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL
P4	3	CLK1	FERR#	FERR#
P4	7	D15	D31#	D31-00
P4	9	D14	D30#	D31-00
P4	11	D13	D29#	D31-00
P4	13	D12	D28#	D31-00
P4	15	D11	D27#	D31-00
P4	17	D10	D26#	D31-00
P4	19	D9	D25#	D31-00
P4	21	D8	D24#	D31-00
P4	23	D7	D23#	D31-00
P4	25	D6	D22#	D31-00
P4	27	D5	D21#	D31-00
P4	29	D4	D20#	D31-00
P4	31	D3	D19#	D31-00
P4	33	D2	D18#	D31-00
P4	35	D1	D17#	D31-00
P4	37	D0	D16#	D31-00

Table 9. Pentium II Processor Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL
P5	3	CLK1	FRCERR	FRCERR
P5	7	D15	D47#	D63-32
P5	9	D14	D46#	D63-32
P5	11	D13	D45#	D63-32
P5	13	D12	D44#	D63-32
P5	15	D11	D43#	D63-32
P5	17	D10	D42#	D63-32
P5	19	D9	D41#	D63-32
P5	21	D8	D40#	D63-32
P5	23	D7	D39#	D63-32
P5	25	D6	D38#	D63-32
P5	27	D5	D37#	D63-32
P5	29	D4	D36#	D63-32
P5	31	D3	D35#	D63-32
P5	33	D2	D34#	D63-32
P5	35	D1	D33#	D63-32
P5	37	D0	D32#	D63-32

Table 9. Pentium II Processor Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL
P6	3	CLK1	IERR#	IERR#
P6	7	D15	D63#	D63-32
P6	9	D14	D62#	D63-32
P6	11	D13	D61#	D63-32
P6	13	D12	D60#	D63-32
P6	15	D11	D59#	D63-32
P6	17	D10	D58#	D63-32
P6	19	D9	D57#	D63-32
P6	21	D8	D56#	D63-32
P6	23	D7	D55#	D63-32
P6	25	D6	D54#	D63-32
P6	27	D5	D53#	D63-32
P6	29	D4	D52#	D63-32
P6	31	D3	D51#	D63-32
P6	33	D2	D50#	D63-32
P6	35	D1	D49#	D63-32
P6	37	D0	D48#	D63-32

Table 9. Pentium II Processor Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL
P7	3	CLK1	STPCLK#	STPCK#
P7	7	D15	A15#	A31-00
P7	9	D14	A14#	A31-00
P7	11	D13	A13#	A31-00
P7	13	D12	A12#	A31-00
P7	15	D11	A11#	A31-00
P7	17	D10	A10#	A31-00
P7	19	D9	A09#	A31-00
P7	21	D8	A08#	A31-00
P7	23	D7	A07#	A31-00
P7	25	D6	A06#	A31-00
P7	27	D5	A05#	A31-00
P7	29	D4	A04#	A31-00
P7	31	D3	A03#	A31-00
P7	33	D2	A02# tied high	A31-00
P7	35	D1	A01# tied high	A31-00
P7	37	D0	A00# tied high	A31-00

Table 9. Pentium II Processor Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL
P8	3	CLK1	A20M#	A20M#
P8	7	D15	A31#	A31-00
P8	9	D14	A30#	A31-00
P8	11	D13	A29#	A31-00
P8	13	D12	A28#	A31-00
P8	15	D11	A27#	A31-00
P8	17	D10	A26#	A31-00
P8	19	D9	A25#	A31-00
P8	21	D8	A24#	A31-00
P8	23	D7	A23#	A31-00
P8	25	D6	A22#	A31-00
P8	27	D5	A21#	A31-00
P8	29	D4	A20#	A31-00
P8	31	D3	A19#	A31-00
P8	33	D2	A18#	A31-00
P8	35	D1	A17#	A31-00
P8	37	D0	A16#	A31-00

Table 9. Pentium II Processor Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL
P9	3	CLK1	SMI#	SMI#
P9	7	D15	RSP#	RSP#
P9	9	D14	RP#	RP#
P9	11	D13	DEP7#	DEP
P9	13	D12	DEP6#	DEP
P9	15	D11	DEP5#	DEP
P9	17	D10	DEP4#	DEP
P9	19	D9	DEP3#	DEP
P9	21	D8	DEP2#	DEP
P9	23	D7	DEP1#	DEP
P9	25	D6	DEP0#	DEP
P9	27	D5	AP1#	AP#
P9	29	D4	AP0#	AP#
P9	31	D3	A35#	A35-32
P9	33	D2	A34#	A35-32
P9	35	D1	A33#	A35-32
P9	37	D0	A32#	A35-32

Table 9. Pentium II Processor Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL
P10	3	CLK1	LINT1/NMI	LINT1, NMI**
P10	7	D15	RS2#	RS#
P10	9	D14	RS1#	RS#
P10	11	D13	RS0#	RS#
P10	13	D12	TRDY#	TRDY#
P10	15	D11	DRDY#	DRDY#
P10	17	D10	DBSY#	DBSY#
P10	19	D9	AERR#	AERR#
P10	21	D8	BERR#	BERR#
P10	23	D7	BINIT#	BINIT#
P10	25	D6	RESET#	RESET#
P10	27	D5	PREQ#	PREQ# **
P10	29	D4	PRDY#	PRDY#
P10	31	D3	BP3#	BP3#
P10	33	D2	BP2#	BP2#
P10	35	D1	BPM1#	BPM1#
P10	37	D0	BPM0#	BPM0#

** These signals are buffered (not latched) in State mode.

Table 9. Pentium II Processor Signal List (Cont.)

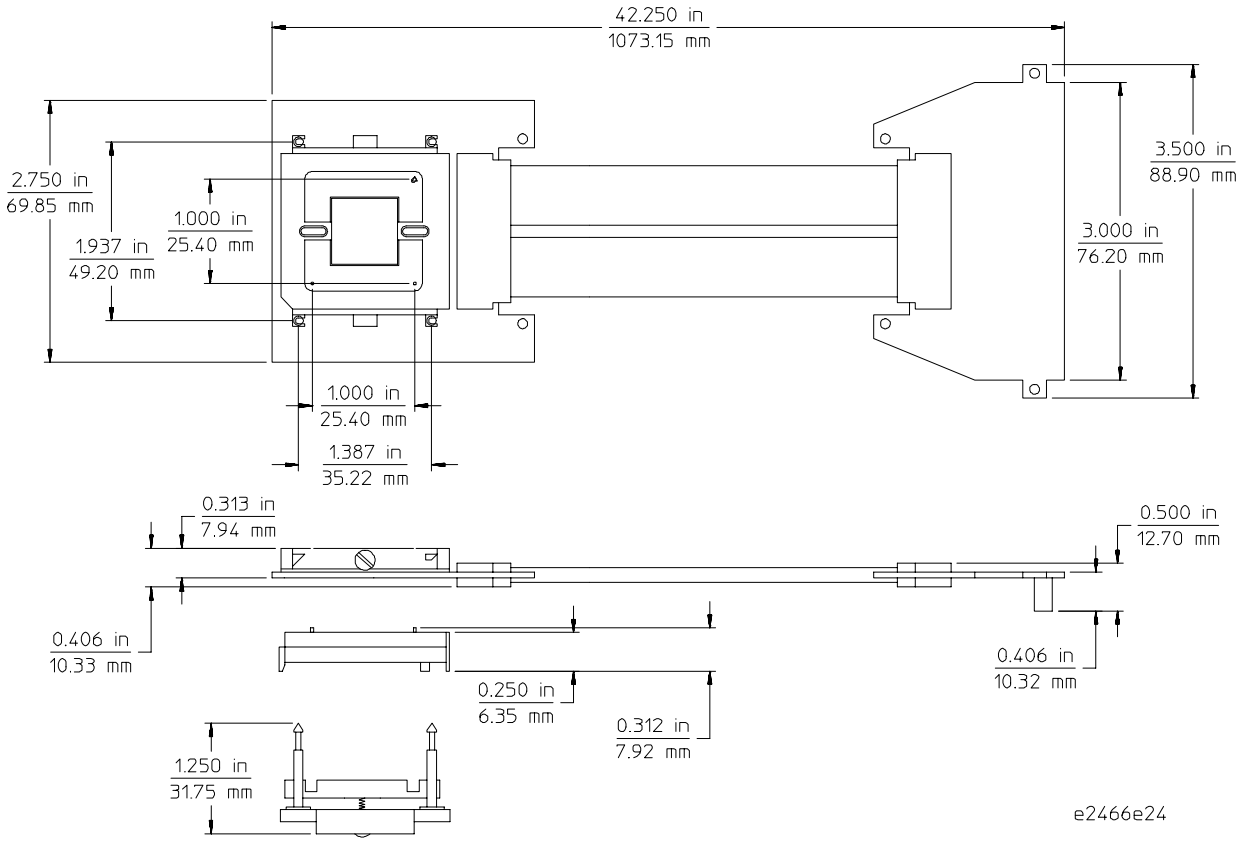
J2 (APIC)					J3 (JTAG)			
Pin #	**Signal**	**Signal**	**Pin #**		**Pin #**	**Signal**	**Signal**	**Pin #**
10	n/c	n/c	9		10	GND	TRST#	9
8	n/c	nc	7		8	GND	TDO	7
6	GND	PICD1#	5		6	GND	TDI	5
4	GND	PICD0#	3		4	GND	TMS	3
2	GND	PICCLK	1		2	GND	TCK	1
Refer to chapter 1 for additional information on connecting to these signals.								

The preprocessor interface captures but does not display the REQ[4:0]# bus signal group.

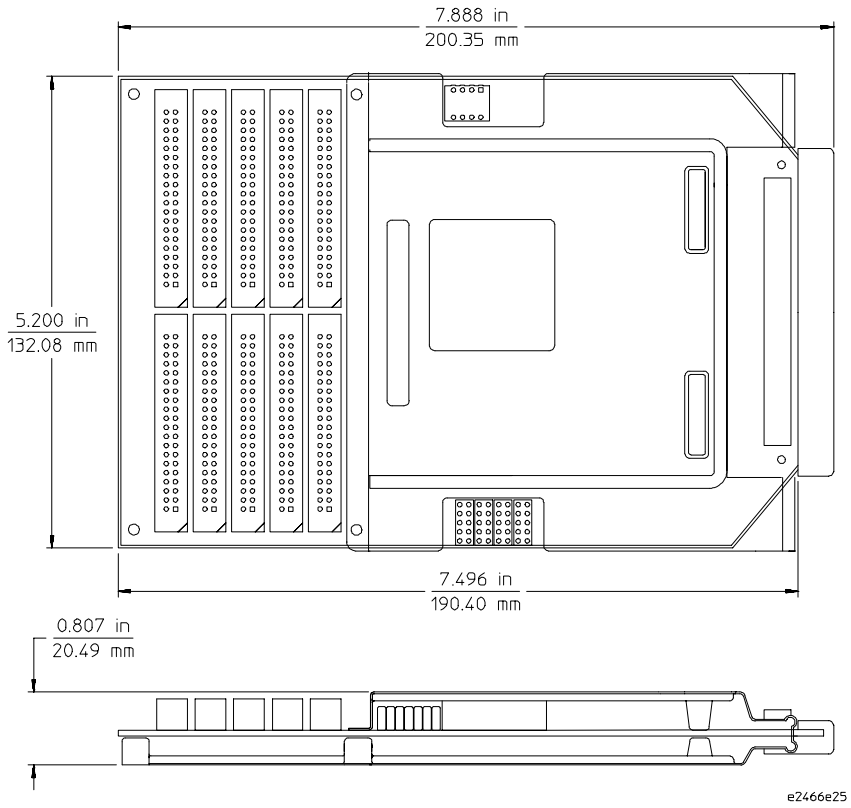
Circuit Board Dimensions

The figure below and on the next page give the dimensions for the preprocessor interface assembly. The dimensions are listed in inches and millimeters.

Figure 22



HP E2466C Dimensions (part 1 of 2)



HP E2466C Dimensions (part 2 of 2)

Repair Strategy

The repair strategy for this preprocessor interface is board replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Table 10. Replaceable Parts

HP Part Number	Description
E2466-69509	Preprocessor Interface Circuit Board
E2466-68707	Software disk pouch
E2466-61601	Probe Cable
E2466-61201	Alignment Clamp
E2466-63201	Interposer Adapter
E2466-68501	Fan and Heat Sink Assembly

A

If You Have a Problem

If You Have a Problem

Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Hewlett-Packard service center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and preprocessors. Otherwise, you may damage circuitry in the analyzer, preprocessor, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reconnect all cables and probes, ensuring that there are no bent pins on the preprocessor interface or poor probe connections.**
- ☐ **Check that the logic analyzer threshhold is set for TTL levels.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive Loading" in this chapter for information on other sources of intermittent data errors.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and preprocessor interface connections.
- ☐ Check for bent or damaged pins on the preprocessor probe.

No trace list display

If there is no trace list display, it may be that your analysis specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your analysis sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Preprocessor Problems

This section lists problems that you might encounter when using a preprocessor. If the solutions suggested here do not correct the problem, you may have a damaged preprocessor. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the preprocessor interface, the microprocessor (if socketed) or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the preprocessor and target system.**

  1 Power up the analyzer and preprocessor.

  2 Power up the target system.

  If you power up the target system before you power up the preprocessor, interface circuitry in the preprocessor may latch up and prevent proper target system operation.

- ☐ **Verify that the microprocessor and the preprocessor interface are properly rotated and aligned, so that the index pin on the microprocessor (such as pin 1 or A1) matches the index pin on the preprocessor interface.**

- ☐ **Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and are firmly inserted.**

- ☐ **Reduce the number of extender sockets.**

See Also "Capacitive Loading" in this appendix.

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and transaction tracker failures.

- **Ensure that the preprocessor operating mode switches are correctly set for the measurement you are trying to make.**
- **Do a full reset of the target system before beginning the measurement.**

  Some preprocessor designs require a full reset to ensure correct configuration.
- **Ensure that your target system meets the timing requirements of the processor with the preprocessor probe installed.**

  See “Capacitive Loading” in this chapter. While preprocessor loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.
- **Ensure that you have sufficient cooling for the microprocessor.**

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the preprocessor interface, or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz, or that have fast edge speeds.

Transaction Tracker/Inverse Assembler Problems

This section lists problems that you might encounter while using the transaction tracker/inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the preprocessor or in your target system. If you follow the suggestions in this section to ensure that you are using the preprocessor and transaction tracker/inverse assembler correctly, you can proceed with confidence in debugging your target system.

No transaction tracking or incorrect transaction tracking

- **Ensure that each logic analyzer pod is connected to the correct preprocessor connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and preprocessor cable numbers. Preprocessors must supply address, data, and status information to the analyzer in a predefined order. The cable connections for each preprocessor are often altered to support that need. Thus, one preprocessor might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 1 for connection information.

- **Check the activity indicators for status lines locked in a high or low state.**

- **Verify that the A[35:32], A[31:00], D[63:32], D[31:00], STAT_1, and STAT_0 format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. See Chapter 2 for more information.

- **Verify that storage qualification has not excluded storage of all the needed transaction phase information.**

Transaction tracker/inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **Ensure that the transaction tracker/inverse assembler is on the same disk as the configuration files you are loading and is in the same directory on the HP 16500B/C mainframe. For the HP 16505A Prototype Analyzer the transaction tracker must be in the /hp16505/ia directory.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding transaction tracker/inverse assembler for the Pentium II processor. If you delete the transaction tracker/inverse assembler file or rename it, the configuration process will fail to load the transaction tracker/inverse assembler file properly.

  See Chapter 1 for details.

Transaction tracker/inverse assembler errors and warnings

********** ******** (no data displayed in the transaction display)**

It is common for transactions near the end of the acquisition to be clipped such that not all data phases are captured. In this case, any data states which are missing will be indicated by a row of asterisks.

? (appears next to a disassembled instruction)

Branch Trace Messages normally guarantee accurate disassembly. Intel has acknowledged a BTM anomaly in the Pentium II processor where the current BTM target address is okay, but the next BTM causing address is incorrect. The HP 16505A software attempts to work around this problem when performing instruction disassembly, but in some cases may not be able to, in which case it marks the instruction with a question mark. This questionable instruction may have been prefetched but not executed.

<ia notice: long format requires Intel NDA>
<ia notice: non-ReqA info requires Intel NDA>

The features you have tried to access are only available in the restricted version of the HP E2466C. Contact your HP Sales Office for information on obtaining the appropriate Intel non-disclosure forms and software for accessing the restricted features.

<pp error: h/w in timing mode or clk qual off>

One of the following conditions exist:

- The Preprocessor Interface hardware switches and the logic analyzer are set to different modes (one State and one Timing).
- The master clock is not set to (L↑)*(M=0) in the HP 16505A Format window. Note that the clock qualifier must always be used, and storage qualification is not allowed in the trigger specification for proper transaction tracker/inverse assembler operation.
- The logic analyzer cables are not connected properly to the preprocessor interface.

<pp error: sync lost -- reset target>
<pp error: rcnt invalid -- reset target>
<pp error: scnt invalid -- reset target>

The preprocessor interface hardware tracks the processor bus from reset. If the logic analyzer is turned off while the target is on, or if the preprocessor switches are changed while the target is on, synchronization with the processor bus is lost. To correct this error, reset the target.

<ia error: BTM with target code read missing>

Because disassembly was selected in Preferences dialog, instructions would normally be displayed for the current Branch Trace Message transaction. If the next BTM was found, but the code read at the branch target address for the current BTM is missing, then this error results. To correct this error, disable all processor instruction caches.

<ia warning: too few states -- modes assumed>

The preprocessor interface communicates its switch settings and dynamic AERR/BINIT observation policies to the logic analyzer via a repeating serial frame on the preprocessor-generated "config" signal. This error indicates that not enough states were acquired by the logic analyzer to contain a full serial frame. The software makes the assumptions listed below.

-- State Mode with Compacted Clock Qualifier

-- AERR/BINIT observation policies disabled

<ia warning: next BTM missing -- no disassembly>

Disassembled instructions are displayed as a continuous block for each Branch Trace Message (BTM) transaction. For any given BTM, the software searches for the next BTM to determine which instruction caused a branch to be taken. Near the end of acquisition, the next BTM may be incomplete or missing. Also, if the number of states to the next BTM exceeds the internal search limit, it will be treated as missing.

<ia warning: disassembly requires Branch Trace>

With "Display Disassembly" selected in the Preferences dialog, a code read from the reset vector is treated as a "virtual" Branch Trace Message and normally begins a block of disassembled instructions. This warning indicates that the next "real" BTM is not found. To correct this warning, turn off "Display Disassembly" or enable BTMs on the target system.

<data ECC error: ... >

"Display Read/Write ECC Errors" is selected in the Preferences dialog and an error was detected on D[63:00]# or DEP[7:0]#. This could be a real data integrity problem on the target system, but other more likely reasons are listed below:

-- E2466C probe end not clamped tightly to CPU daughter card.

-- Logic analyzer pods for the D[63:00]# signals are swapped.

-- Data bus ECC checking is not enabled on the target system.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms another measurement module, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

Logic Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the Pentium II processor transaction tracker/inverse assembler that is attached to the configuration file. Ensure that the transaction tracker/inverse assembler file is not renamed or deleted.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly for the HP 16550B cards. Ensure that your cable connections match the silk screening on the card. Then, repeat the measurement.

See Also The *HP 16550B Logic Analyzer Service Guide*.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ **Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500B/C disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.**

See Also Chapter 1 describes how to load configuration files.

“Selected File is Incompatible”

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

“Slow or Missing Clock”

- This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500B/C or HP 16501A frame. Ensure that the cards are firmly seated.
- This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the preprocessor interface. See Chapter 1 to determine the proper connections.

"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

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Hewlett-Packard
P.O. Box 2197
1900 Garden of the Gods Road
Colorado Springs, CO 80901

About this edition

This is the first edition of the *HP E2466C Preprocessor Interface for the Pentium® II Processor User's Guide*. Edition dates are as follows:

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New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by you. The dates on the title page change only when a new edition is published.

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